A High Level Hardware Design Language SV+

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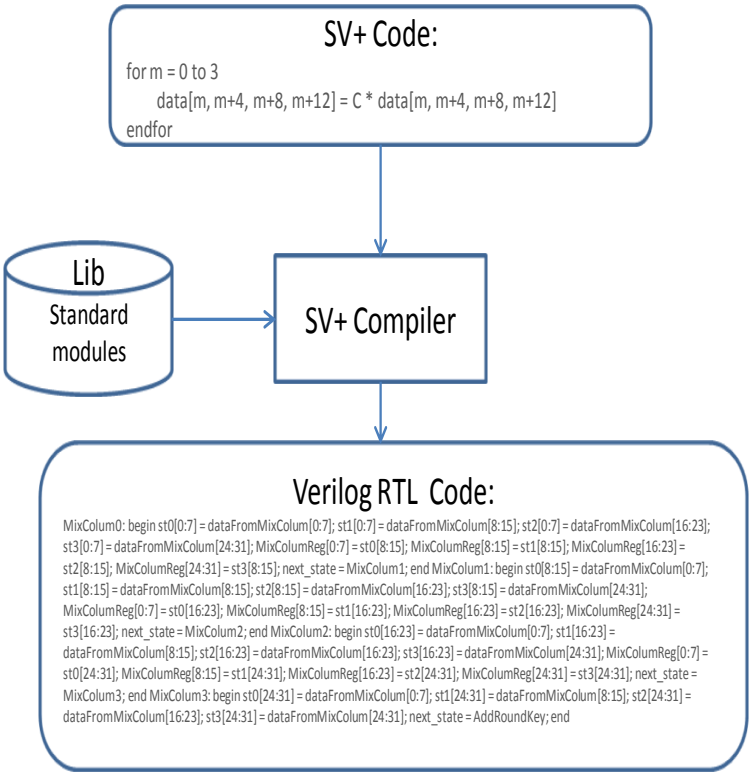

Design a high level language SV+ as well as the compiler that compiles the SV+ code into Verilog RTL code